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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,760	06/15/2001	Shuo-Yen Robert Li	Li7	1794

570 7590 11/29/2006

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EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,760	LI ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,11 and 23* is/are allowed.

6)☒ Claim(s) *1-7,9,12-18,20-22 and 24* is/are rejected.

7)☐ Claim(s) *8,19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 12, 21, 24, 2, 13, 3, 14, 4, 15, 22, 5, 16, 6, 17, 7, 18, 9, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMillen (US 4623996) in view of Simpkins et al. (US 6931002 B1).

Regarding claims 1, 12, 21, 24, McMillen discloses implicitly the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Fig. 1, recited elements "a plurality of input ports 21' as M input; and "a plurality of output ports 25" as N output ports; column 5, lines 35 – 59), the switch comprising an input module (Fig. 1, recited elements "a plurality of input ports 21' as input module), having M inputs and B outputs, B>M, for switching the M input packets to M of the B outputs to produce M switched packets during each of the frame times (recited " input ports 21" as M inputs, and queue selectors 22 has a plurality of outputs" as B output; column 5, lines 37 – 43), a packet buffer including B registers, coupled to the input module, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets (recited " queue selector 21 having a plurality of outputs individually coupled to separate queues of a corresponding queue set" as buffer including B registers, coupled to the

input module; column 5, lines 32 – 43), and an output module ("a plurality of output ports 25" as N output ports; column 5, lines 35 – 59) , having B inputs and N outputs coupled to the packet buffer (Fig. 1, recited "a plurality of output ports" as N outputs, and "each of the output arbitrator has a plurality of inputs" as B inputs; column 5, lines 32 – 37), for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets (column 5, lines 48 – 59). However, McMillen does not teach explicitly M input packets arriving in each of a sequence of frames times to N output ports, storing the M switched packets into M available registers during each of the frame times to produce M stored packets, and transferring up to N packets from occupied registers to each of the frame times to the output ports based upon destination addresses contained within each of the stored packets. Simpkins et al. disclose explicitly M input packets arriving in each of a sequence of frames times to N output ports (recited "sequentially receives the data from the input ports, and switches a sequentially received data from a respective input port to a respective output Port" as M input packets arriving in each of a sequence of frames times to N output ports; column 3, lines 44 – 49, Fig. 5), storing the M switched packets into M available registers during each of the frame times to produce M stored packets (recited "storing the TDM data in a preselected area of a shared memory" as storing the M switched packets into M available registers during each of the frame times; column 3, lines 54 – 59), and transferring up to N packets from occupied registers to each of the frame times to the output ports based upon destination addresses contained within each of

the stored packets (recited "reading the TDM data from the preselected area of said shared memory; and transmitting the TDM data from the output port; column 3, lines 60 – 66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McMillen to include M input packets arriving in each of a sequence of frames times to N output ports, storing the M switched packets into M available registers during each of the frame times to produce M stored packets, and transferring up to N packets from occupied registers to each of the frame times to the output ports based upon destination addresses contained within each of the stored packets such as that taught by Simpkins et al. in order to provide a hybrid switch for switching both TDM data and packet data, where the switching of packet data has no effect on the latency or jitter of the switching of TDM data (as suggested by Simpkins et al., see column 3, lines 23 – 26).

Regarding claims 2, 13, McMillen discloses the limitation of the packet switch as recited in claim 1 wherein the input module is an MxB crossbar switch (Fig 1, Fig. 1, recited elements "a plurality of input ports 21' as M input, and queue selectors 22 has a plurality of outputs" as B output; column 5, lines 35 – 47).

Regarding claims 3, 14, McMillen discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Fig. 1, recited elements "a plurality of input ports 21' as M input; and "a plurality of output ports 25" as N output ports; column 5, lines 35 – 59), McMillen does not disclose expressly the packet switch as recited in claimed wherein the packet buffer is a one-stop shared buffer memory. Simpkins et al. disclose the limitation of the

packet switch as recited in claimed wherein the packet buffer is a one-stop shared buffer memory (recited "a shared memory, and in a shared memory packet switch, a large common block of random access memory (RAM) is used to store all packets awaiting transmission. Individual queues of packets, each associated with a single output logical port, are maintained in the shared memory" as buffer is a one-stop shared buffer memory; column 6, line 20 – 28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McMillen to include packet switch as recited in claimed wherein the packet buffer is a one-stop shared buffer memory such as that taught by Simpkins et al. in order to provide a hybrid switch for switching both TDM data and packet data, where the switching of packet data has no effect on the latency or jitter of the switching of TDM data (as suggested by Simpkins et al., see column 3, lines 23 – 26).

Regarding claims 4, 15, 22, McMillen discloses the limitation of the packet switch as recited in claimed further including queues and their identifiers to store the destination addresses (recited " routing tag signal" as destination address; column 6, lines 56 – 64) and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$ (column 7, lines 6 – 8).

Regarding claims 5, 16, McMillen discloses the limitation of the packet switch as recited in claimed further including a register selector (recited "queue selector" as

register selector) for assigning the M of the B registers during each of the frame times to generate M assigned registers (Fig. 2, column 6, lines 44 – 49).

Regarding claims 6, 17, McMillen discloses the limitation of the packet switch as recited in claimed further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues based upon destination information in the header information of the packets (column 6, lines 48 – 59), but not from the M header hoppers. Simpkins et al. discloses the limitation of stored switch configuration (recited "stored switch configuration" as header hoppers coupled to the input module, see Fig. 6, element 35, and element 42 the connection bus; column 5, lines 36 – 41), for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times (recited "for each memory input cycle of the shared memory 40, if the input time slot belongs to a TDM logical port, the address of the shared memory 40 is selected from the TSI control function 43. If the input time slot belongs to a packet logical port, the address of the shared memory 40 is selected from the packet switch control function 44. The TSI control function 43 always generates the same memory address during the cycle corresponding to a particular time slot of a frame"; column 7, lines 26 – 41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McMillen to include header hoppers coupled to the input module, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times such as that taught by

Simpkins et al. in order to provide a hybrid switch for switching both TDM data and packet data, where the switching of packet data has no effect on the latency or jitter of the switching of TDM data (as suggested by Simpkins et al., see column 3, lines 23 – 26).

Regarding claims 7, 18, McMillen discloses the limitation of the packet switch as recited in claimed further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues based upon destination information in the header information of the packets (column 6, lines 48 – 59), but not from the M header hoppers. Simpkins et al. discloses the limitation of stored switch configuration (recited "stored switch configuration" as header hoppers, see Fig. 6, element 35, column 5, lines 36 – 41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McMillen to include the header hoppers such as that taught by Simpkins et al. in order to provide a hybrid switch for switching both TDM data and packet data, where the switching of packet data has no effect on the latency or jitter of the switching of TDM data (as suggested by Simpkins et al., see column 3, lines 23 – 26).

Regarding claims 9, 20, McMillen discloses the limitation of the packet switch as recited in claimed wherein each of the B registers is a circular shift register (recited "round robin priority scheme" as a circular shift register; column 7, lines 16 – 17).

Allowable Subject Matter

3. Claims 10, 11, 23 are allowed over prior art.

Claims 8, 19, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed on 7/21/2006 with respect to claims 1 – 24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ACL

Nov 22, 2005

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